Code No.: 10605/20605

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)
Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist). Hyderabad

III B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, DECEMBER-2019

Subject: WEB TECHNOLOGIES

Branch: CSE

Time:	3 hours	Max. Marks: 75
Answer any 5 questions of the following 5x15		5x15M=75 M
1.	a) Explain how a basic table is created using HTML.b) Explain basic formatting tags.	[7M] [8M]
2.	a) How do you get JavaScript onto a web page? Explain with examples?b) Write a function in java script that validates if the content has the general system.	[9M] ntax of an email? [6M]
3.	a) Write XML database with details of student (Rollnum, Name(first_name) name(First_name, Last_name) branch, year, address (Door_No, Street, and write DTD to validate the above XML file.	City), Email, Ph.No. [7M]
4.	b) Explain How XML schema is better than DTD.a) What are the advantages of JAVA beans?b) Explain about Bean info interface.	[8M] [7M] [8M]
5.	a) Write a servlet program to display form details when you click on subn b) Explain the core interface provided in javax.servlet.http package.	nit button. [9M] [6M]
6.	Discuss JSP Application design with MVC set up and JSP environment.	
7.	a) Develop a JSP to detect the web browser.b) Explain JSP scripting components with examples.	[6M] [9M]
8.	a) Explain about Javax.sql.* package.b) Explain different types of JDBC drivers with a neat sketch.	[6M] [9M]

Code No.: 20519

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III B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, DECEMBER-2019

Subject: **SOFTWARE TESTING METHODOLOGIES**

Branch: CSE

Answer ANY FIVE questions of the following 5x15M= 75M	
1. a) Explain model for testing.	[7M]
b) Compare and contrast between testing versus Debugging. [8	8M]
2. a) Discuss about control flow graphs. What are difference between control flow	
graphs and flow charts. [8	8M]
b) Why All-du-Paths (ADUP) is the strongest data-flow testing strategy?	7M]
3. a) What are the transaction flows? Discuss their complications.	7M]
b) Compare the transaction testing strategies with the data- flow testing.	8M]
4. a) How programmers and testers treat Ugly Domains? [9]	9M]
b) Explain the acronym Closed Off Outside, Open Off Inside (COOOOI) in domain	n
testing.	[6 M]
5. a) Explain the procedure used in testing loops in path testing.	9M]
b) Explain the terms paths, nodes and links.6. a) What is decision table and how does it is useful in testing. Explain it with help of	6M] f
	9M]
b) Explain about K V chats with suitable examples. Discuss their applications.	6M]
7. a) What are the types of bugs that can cause state graphs.	7M]
b) What are principles of state testing? Explain its advantage and disadvantages. [8]	M]
8. a)Explain in detail performance testing.	8M]
b) Discuss about the partitioning algorithm	[7M]

Code No.: 20521

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

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III B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, DECEMBER-2019

Subject: **COMPILER DESIGN**

Branch: CSE

Time: 3 hours

Max. Marks: 75

Answer any 5 questions of the following

5x15M=75 M

1. a) List the differences between compiler, interpreter and assembler

[7M]

b) Discuss about specification of tokens in detail

[8M]

2. a) Explain basic steps to construct recursive decent parser

[10+5M].

b) Writ the psecudo code for the following grammar

 $E \rightarrow num T$

 $T \rightarrow * num T/\varepsilon$

3. Consider the following grammar

 $S \rightarrow Aa$

 $S \rightarrow bAc$

 $S \rightarrow dc$

 $S \rightarrow bda$

 $S \rightarrow d$

Discuss the LALR parsing method for this grammar list out canonical collections and also construct a parsing table.

4. a) Explain about implicit and explicit type conversions

[7M]

b) Construct the syntax tree for the expression x*y-5+z

[8M]

- 5. Explain various data structures used to implement the symbol table.
- 6. Explain different loop optimization techniques.
- 7. What is a flow graph? Explain how a given program is converted into a flow graph with an illustrative example.
- 8. Explain about Register Allocation and Assignment in detail